

Abhilash Joyeal Uppalaguptha

abhilashjoyealuppalaguptha@gmail.com | [Github](#) | [LinkedIn](#)

SUMMARY

Driven Electronics & Communication Engineering student focused on VLSI design, embedded systems, and hardware innovation. Actively building projects at the intersection of AI, FPGA/Verilog, and real-world problem solving.

President of the OPTICA Student Chapter, leading initiatives in deep tech. Passionate about developing defense-grade and socially impactful systems, including safety tech and autonomous platforms.

TECHNICAL SKILLS

Core Domains

- VLSI Design
- IoT & Embedded Systems
- Full Stack

Programming & Hardware

- Verilog.
- C, Python, HTML,CSS, MATLAB.
- ESP32, Microcontrollers
- Raspberry Pi, Developing simple robots.

Tools & Platforms

- Cadence
- MATLAB
- PCB Design

Leadership & Execution

- Public Speaking
- Team Leadership
- Startup Strategy

PROFESSIONAL EXPERIENCE

OPTICA Student Chapter, President

Feb 2025 - Present

- Leading the student chapter focused on photonics, optics, and advanced technologies.
- Organizing technical events, workshops, and knowledge sessions to increase domain engagement.
- Driving initiatives to connect students with research and innovation opportunities.

Core Team Member, Entrepreneurship Development Cell

July 2025 - Present

- Contributing to planning and execution of large-scale entrepreneurial events like Creathon and E-Summit.
- Supporting startup incubation activities, including idea validation and pitching strategies.
- Collaborating with leadership teams to expand student participation and outreach.

NAVIEL (Startup Initiative), Founding member

Jan 2026 - Present

- Worked on creating better hardware for safety and safer solutions for citizen safety and also working on multidisciplinary ideas as a startup initiative
- Contributed to designing tech and innovation that common people need.
- Collaborated in a team environment to build and refine innovative solutions

EDUCATION

Bachelor of Technology, Electronics & Communication Engineering

2024-2028

Aditya University

Class 12 (Intermediate), MPC

2022-2024

Narayana Junior College

PROJECTS

BitFlow RTL Coding Platform

- For increasing demand of RTL Design Engineers, I created a platform for RTL Coding(Verilog/SystemVerilog).
- Designed a software platform which is reliable & industry.
- Focused on real-time systems and scalability.

[Link](#)

Trana-Trace (Core VLSI Project)

[Link](#)

- Developed a chip system which helps in mobile security in times of mobile theft & battery drain.
- Designed the entire VLSI architecture using FSM concepts in Verilog.
- Learnt real time workflow different technologies from VLSI to IoT to Web development.

ADDITIONAL SKILLS, EXTRA CURRICULARS & AWARDS, ACHIEVEMENTS

Public Speaking Winner in various competitions

- Viksit Bharat speech competition won at district level, upto State Level participation.
- Achieved many prizes in Public speaking in University.